DWG ISSUE	EE OR CD ISSUED	DATE ISSUE	[illegible]	APPD
1	—	10-8-74	LRE LRE	RWF MTS RFG
2D1	—	1-5-76	APPL LRE	JLT LEG RFG

SHEET INDEX

CONTENTS	SHEET NO.	SHEET ISSUE
SHEET INDEX SYMBOL RECORD OF CNANGES NOTES USED-ON TABLE SUPPORTING INFORMATION CURRENT DRAIN	1	2
CIRCUIT SCHEMATIC	2	2
COMPDNENT LIST CIRCUIT DESCRIPTIDN	3	2

SYMBOL

BUFFER C
ELEMENT IDENT
A

TERM. MOD.	FUNCT	TERM.	LOC
CLKITRO	I	015	2A3
ENDTO	I	104	2AC
LDITR1	I	004	2A6
LØADO	I	106	2A7
SDITRO	I	002	2A0
SNIFT1	I	014	2A3
PN4S	I	217,317	2A9
LDDO	Ø	017	2G9
LOD1	Ø	115	2G9
PPEHO	Ø	103	2N3
PPELO	Ø	114	2H7
-17.20V	Ø	0T8,1T8	2G9
INFPHO	ØI	101	2N3
INFPLO	ØI	005	2H6
INF000	ØI	116	2H6
INF010	ØI	216	2H6
INF02D	ØI	016	2N5
INF030	ØI	31S	2H5
INF04D	ØI	113	2H4
INF05D	ØI	21S	2H4
INF060	ØI	013	2H4
INFD70	ØI	214	2H4
INF080	ØI	006	2N2
INF090	ØI	207	2H2
INF100	ØI	105	2H2
INF110	ØI	305	2N2
INF120	ØI	003	2H1
INF130	ØI	203	2N1
INF140	ØI	102	2N1
INF150	ØI	301	2H0
+5	P	000,119	2G7
GRD	G	200,319	2G8

RECORD DF CHANGES

DWG ISS	PREV FURN	STD	MFR DISC	SEE NDTE

SYSTEM USED DN	DESIGN CONTROL
COMMON SYSTEMS	IN

CURRENT DRAIN: +5V SUPPLY = 325mA
-48V SUPPLY = 50mA

NOTES:

1. ⏚ GROUND RETURN

2. UNLESS DTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN DHMS
CAPACITANCE VALUES ARE IN MICRDFARADS
VALUES PRECEDED BY THE SYMBOL +(PLUS)
OR -(MINUS) ARE IN VOLTS

3. BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS

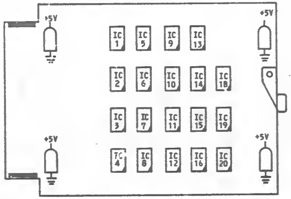
IC CODE	BAT. TERM.	GRD TERM.
41AE	16	7,8
41BP	16	8
41CA	16	8
41CF	16	7,8
41DA	16	7,8
41EF	16	8

4 BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
+S	000,119
GRO	200,319

5. HORIZONTAL MOUNTING CENTERS AT 0.50 INCN.

6. INTEGRATED CIRCUIT LOCATION GUIDE:
(COMPONENT SIDE SHOWN)



UNMARKED COMPONENTS ARE FILTER CAPACITORS

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK CODE	JK12
CONNECTOR ON FRAME	947C OR 947A
SERIES FOR LATEST CLASS A CHANGE. (ANY NIGHER SERIES IS ACCEPTABLE.	
ACCEPTABLE SERIES	1

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN TNIS DRAWING ONLY THOSE SNEETS AFFECTED WILL BE REISSUED.
2. TNIS SHEET INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACN TIME ANY SHEET OF THE DRAWING IS REISSUED, OR A NEW SHEET IS ADDED.
3. THE ISSUE NUMBER ASSIGNED TO A CHANGED OR NEW SHEET WILL BE THE SAME ISSUE NUMBER AS THAT OF THE FIRST SHEET.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER.
5. THE LAST ISSUE NUMBER OF TNE FIRST SHEET INDEX IS RECOGNIZED AS THE LATEST ISSUE NUMBER OF THE DRAWING AS A WHOLE

NOTICE- NOT FOR USE OR DISCLOSURE OUTSIDE THE BELL SYSTEM EXCEPT UNDER WRITTEN AGREEMENT.

ISSUE
2D1

1N98

JK12 CIRCUIT PACK

BUFFER C
CIRCUIT

②

AT&TCO
STANDARD

CPS-JK12
3 SHEETS

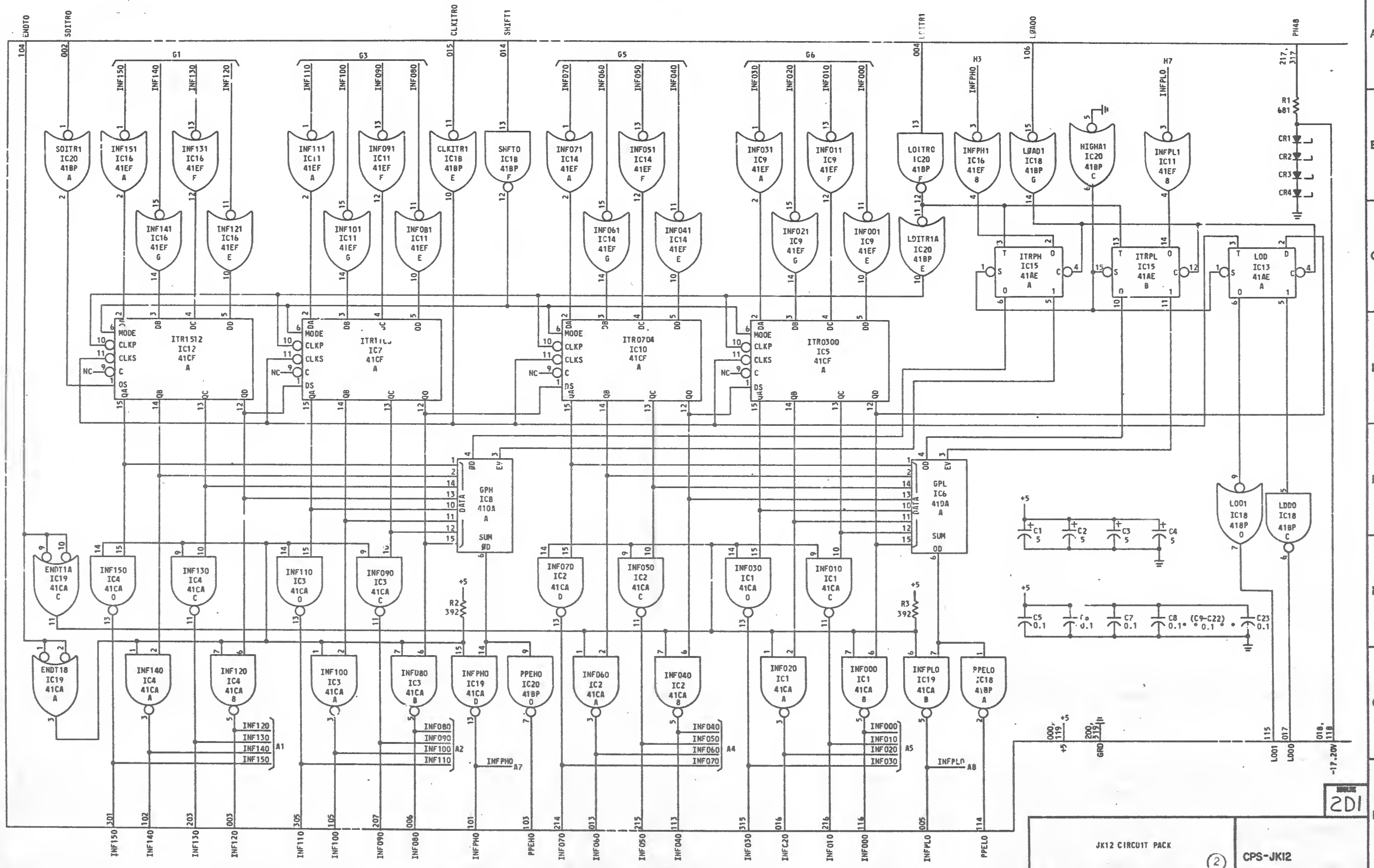
BELL TELEPHONE LABORATORIES
INCORPORATED

6S

CPS-JK12

PART OF CPS JK12

BUFFER C



JK12 CIRCUIT PACK

②

CPS-JK12

SHEET 2

BELL TELEPHONE LABORATORIES
INCORPORATED

GS

2D1

CPS-JK12

PART OF CPS JK12

BUFFER C

COMPONENT LIST

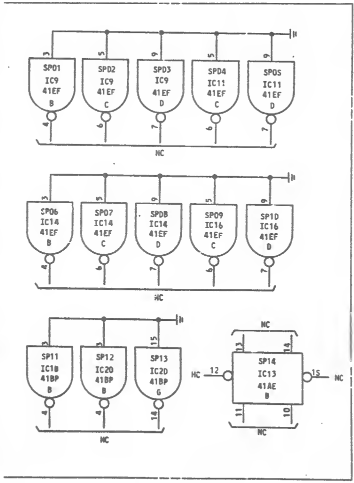
INTEGRATED CIRCUIT

LOC CODE ELEM ID	IC1 41CA		IC2 41CA		IC3 41CA		IC4 41CA		IC5 41CF	
	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A	IHFD20	2G5	IHF06D	2G4	IHF1DD	2G2	IHF140	2G1	ITRD300	2D6
B	IHF000	2G6	IHF040	2G4	IHFDBD	2G2	INF120	2G1		
C	IHFD10	2F6	IHFD50	2F4	IHF090	2F2	INF130	2F1		
D	IHFD3D	2F5	IHFD70	2F4	IHF11D	2F2	IHF1SD	2FD		
E										
F										
G										

LOC CODE ELEM ID	IC6 41DA		IC7 41CF		IC8 41DA		IC9 41EF		IC1D 41CF		IC11 41EF	
	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A	GPL	2E6	ITR1108	2D2	GPH	2E3	IHF031	2BS	ITRD704	2D4	INF111	2B2
B							SPD1	3ED			INFPL1	2B8
C							SPD2	3ED			SP04	3E1
D							SPD3	3E1			SPDS	3E1
E							INFDD1	2C6			INF081	2C3
F							INFD11	2B6			INF091	2B2
G							IHFD21	2CS			IHF101	2C2

LOC CODE ELEM ID	IC12 41CF		IC13 41AE		IC14 41EF		IC1S 41AE		IC16 41EF	
	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A	ITR1512	2D1	LDO	2C9	IHFD71	2B4	ITRPH	2C7	IHF1S1	2BD
B			SP14	3G1	SP06	3FD	ITRPL	2CB	IHFPH1	2B7
C					SP07	3FD			SP09	3F1
D					SP08	3F1			SP1D	3F1
E					INF041	2C4			IHF121	2C1
F					INFDS1	2B4			IHF131	2B1
G					INFD61	,C4			IHF141	2C1

LOC CODE ELEM ID	IC18 418P		IC19 41CA		IC2D 418P	
	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A	PPELD	2G7	EHDT1B	2GO	SDITR1	2BO
B	SP11	3GO	IHFPLD	2G6	SP12	3GO
C	LDDO	2E9	ENDT1A	2FD	HIGHA1	2B8
D	LDD1	2E9	IHFPHO	2G3	PPEHD	2G3
E	CLKITR1	2B3			LDITR1A	2C6
F	SHFTD	2B3			LDITRD	2B6
G	LØAD1	2B7			SP13	3G1



CAPACITOR

DESIGN	CODE
[4]C1-C4	601A,5
[19]CS-C23	KS-19774 L5,D.1

DIODE

DESIG	CODE
[4]CR1-CR4	4488

RESISTOR

DESIG	CODE
R1	KS-146D3 L6,6B1
[2]R2,R3	KS-20616 L1A,392

CIRCUIT DESCRIPTION:

THIS CIRCUIT PACK IS PART OF THE BUFFER UNIT. IT CONTAINS A 16-BIT SHIFT REGISTER FOR PARALLEL-TO-SERIAL AND SERIAL-TO-PARALLEL CONVERSION. TWO 8-BIT PARITY TREES ARE USED TO CHECK AND GENERATE PARITY. THE SERIAL INPUT/OUTPUT LEADS CONNECT TO THE OFF-LINE SERIAL BUFFER ON JK13. PARALLEL INPUT AND OUTPUTS ARE CONNECTED TO THE BIDIRECTIONAL INFORMATION LEADS.

THE REGISTER IS NORMALLY IN THE PARALLEL LOAD MODE. THE MODE INPUT OF THE 41CFs ARE HELD HIGH BY THE SHFT1 INPUT BEING LOW. THE LOADO IS HIGH WHENEVER THE BUFFER UNIT IS NOT IN THE LOAD STATE. IN THIS MODE, THE PARITY F/F ITRPL AND ITRPH ARE HELD IN THE CLEARED STATE. THIS FORCES THE EVEN INPUTS OF THE PARITY TREES GPL AND GPH TO A LOW LEVEL AND THE ODD INPUTS TO A HIGH LEVEL. IN THIS PARITY GENERATION MODE, THE OUTPUTS OF THE PARITY TREES ARE HIGH FOR AN EVEN NUMBER OF ONE INPUTS OR ARE LOW FOR AN ODD NUMBER OF ONE INPUTS. THE TRUTH TABLE BELOW SHOWS THE OPERATION.

Σ OF INPUTS	INPUT EVEN	INPUT ODD	ODD OUT
ODD	D	1	D
EVEN	D	1	1

AN UNLOAD OPERATION IS DEFINED BY A 16-BIT DATA TRANSFER FROM THE OFF-LINE BUFFER TO THE 3A CC. THE FOLLOWING SEQUENCE IS PERFORMED ON JK12.

THE SERIAL DATA FROM THE OFF-LINE BUFFER APPEARS ON SDITRO. LEAD SHIFT1 IS SET HIGH TO PLACE THE 16-BIT REGISTER INTO THE SERIAL SHIFT MODE. SIXTEEN GROUND LEVEL PULSES ARE APPLIED TO LEAD CLKITRD. THE DATA IS SHIFTED INTO THE REGISTER AT THE TRAILING EDGE OF THE CLOCK PULSES. LEAD LDDC IS HELD AT A HIGH LEVEL. THIS MEANS THAT ZERO DATA IS SHIFTED INTO THE OFF-LINE BUFFER DURING UNLOAD OPERATIONS. THE 16-DATA BITS CONTAINED IN THE REGISTER ARE FED INTO THE PARITY TREES. THE PARITY TREES ARE ALLOWED TO SETTLE. THE SHFT1 LEAD IS SET LOW AGAIN TO PLACE THE REGISTER INTO THE PARALLEL LOAD MODE. THE CONTENTS OF THE REGISTER AND THE TWO PARITY BITS ARE THEN GATED ONTO THE INFORMATION BUS LEADS BY SETTING LEAD ENDTD TO A LOW LEVEL.

CIRCUIT DESCRIPTION (CONT):

LOAD

A LOAD OPERATION IS DEFINED BY A 16-BIT DATA TRANSFER FROM THE CC TO THE OFF-LINE BUFFER. THE FOLLOWING SEQUENCE IS PERFORMED ON JK12. WHEN THE LOAD STATE IS SET, LEAD LOADO IS AT GROUND LEVEL REMOVING THE CLEAR INPUT FROM ITRPH, ITRPL, AND LDD1 F/Fs. SIXTEEN BITS OF INFORMATION AND THE TWO PARITY BITS APPEAR IN PARALLEL ON THE INFORMATION BUS LEADS. A SINGLE HIGH LEVEL PULSE APPEARS ON LEAD LDITR1. THE STATE OF THE INFORMATION LEADS IS CLOCKED INTO THE REGISTER AND THE TWO PARITY F/F AT THE TRAILING EDGE OF THE PULSE. IN THE LOAD MODE, THE TWO PARITY TREES AND THE TWO PARITY F/F CHECK FOR PROPER PARITY OF THE JUST RECEIVED DATA WORD. AN ERROR CONDITION IS INDICATED WHENEVER PPELD OR PPEHO IS AT GROUND LEVEL. THE FOLLOWING TRUTH TABLE SHOWS THE CHECKING OPERATION.

Σ OF INPUTS	PARITY BITS	INPUT ODD	INPUT EVEN	ODD OUTPUT	
EVEN	1	D	1	D	NO ERROR
ODD	D	1	D	D	NO ERROR
ODD	1	0	1	1	ERROR
EVEN	D	1	D	1	ERROR

IF AN ERROR CONDITION EXISTS, NO SERIAL SHIFTING INTO THE OFF-LINE BUFFER TAKES PLACE. IF NO ERROR CONDITION EXISTS LEAD SHFT1 IS SET HIGH TO PLACE THE REGISTER INTO THE SERIAL SHIFT MODE. SIXTEEN CLOCK PULSES ON LEAD CLKITRD SHIFT THE 16-BIT WORD INTO THE OFF-LINE BUFFER VIA LEAD LDDO. F/F LDD1 IS CLOCKED ON THE LEADING EDGE OF CLKITRO AND THE REGISTER IS SHIFTED ON THE TRAILING EDGE. THE LDDO F/F KEEPS THE DATA STEADY OVER THE TRAILING EDGE OF THE OFF-LINE SHIFT PULSE ON JK13.

2D1

JK12 CIRCUIT PACK

②

BELL TELEPHONE LABORATORIES
INCORPORATED

6S

CPS-JK12
SHEET 3

PRINTED IN U.S.A.

CPS-JK12